## IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A process comprising:

forming a first dielectric layer on a substrate;

forming a second dielectric layer on the first dielectric layer;

forming a first recess having a first lateral dimension at a bottom portion of the first dielectric layer in contact with the substrate, and having a second lateral dimension at a top portion of the second dielectric layer;

forming a conductive structure in the first recess having vertical sidewalls with the first lateral dimension having a value approximately equal to a value of the second lateral dimension;

first wet etching to expose a first portion of the conductive structure by removing at least a portion of the second dielectric layer;

first rinsing the conductive structure; and

second non-wet etching to expose a second portion of the conductive structure by removing at least a remaining portion of the first dielectric layer and exposing at least a portion of the substrate.

2. (Currently Amended) The process of claim 1, wherein ~~first wet etching includes first etching~~ the second dielectric film includes a polysilicon ~~sacrificial second~~ film ~~that is disposed over the substrate~~.

3. (Currently Amended) The process of claim 1, ~~and~~ wherein first wet etching has ~~is at~~ a rate that is faster than second non-wet etching.

4. (Currently Amended) The process of claim 1, ~~A process comprising:~~

~~forming a first dielectric layer on a substrate;~~

~~forming a second dielectric layer on the first dielectric layer;~~

~~forming a first recess in the first and second dielectric layer to expose a portion of the substrate;~~

~~forming a conductive structure in the first recess;~~

~~first etching to expose a first portion of the conductive structure;~~

~~first rinsing the conductive structure; and~~

~~second etching to expose a second portion of the conductive structure~~

wherein first etching is selected from the group consisting of a wet process and a vapor process, and wherein second etching is selected from the group consisting of a vapor process and a dry process.

5. (Previously Presented) The process of claim 1, wherein the substrate includes a single dielectric stack, wherein first wet etching is selected from the group consisting of a wet process and a vapor process, wherein second non-wet etching is selected from the group consisting of a vapor process and a dry process, and wherein the single dielectric stack is selected from the group consisting of undoped spin-on dielectric, undoped vapor-deposited dielectric, doped spin-on dielectric, and doped vapor-deposited dielectric.

6. (Previously Presented) The process of claim 1, wherein the substrate includes a single dielectric stack, wherein first wet etching is selected from the group consisting of a wet process and a vapor process, wherein second non-wet etching is selected from the group consisting of a vapor process and a dry process, and wherein the single dielectric stack is selected from the group consisting of spin-on undoped silica, spin-on doped silica, borophospho silicate glass, borosilicate glass, phospho silicate glass, doped oxide from the decomposition of tetraethyl ortho silicate, and undoped oxide from the decomposition of tetraethyl ortho silicate.

7. (Canceled)

8. (Currently Amended) The process of claim 1, wherein forming a first recess includes forming the recess in a dielectric first film that is disposed above the substrate, and in a ~~sacrificial~~ second film that is disposed above and on the dielectric first film.

9-71. (Canceled)

72. (New) The process of claim 1, wherein first wet etching includes a first etch chemistry, wherein second non-wet etching includes a second etch chemistry different from the first etch chemistry.

73. (New) The process of claim 1, wherein the first wet etching exposes a first portion of the conductive structure by removing all of the second dielectric layer.

74. (New) The process of claim 1, wherein the first wet etching exposes a first portion of the conductive structure by removing all of the second dielectric layer and exposing at least a portion of the substrate.

75. (New) The process of claim 1, wherein the second dielectric layer further includes a polysilicon layer selected from the group consisting of undoped polysilicon, and heavily doped polysilicon.

76. (New) The process of claim 1, wherein the conductive structure is coupled to a substrate active area.

77. (New) The process of claim 1, wherein the conductive structure includes a container capacitor.

78. (New) The process of claim 1, further including forming a storage cell plate over the conductive structure.

79. (New) The process of claim 1, wherein the conductive structure is formed to extend above a remaining portion of the first dielectric stack to form an exposed vertical portion not in contact with dielectric.

electrically isolating the conductive structure.